CLAIMS

What is claimed is:

1. A method comprising:
forming a first interconnect structure on one side of a first wafer;
forming a number of vias, each of the vias extending through the first interconnect structure and into the first wafer;
depositing an insulating material in each of the number of vias, the insulating material in each via forming an insulating plug;
forming a second interconnect structure over the insulating plugs and the first interconnect structure, wherein each of the insulating plugs extends to one of a number of conductors in the second interconnect structure;
bonding the first wafer to a second wafer to form a wafer stack; and
thinning an opposing side of the first wafer to expose the insulating plug within each of the vias.

2. The method of claim 1, further comprising performing alignment of the wafer stack using the exposed insulating plugs and vias.

3. The method of claim 1, further comprising depositing a layer of dielectric material over the opposing side of the first wafer and the exposed insulating plugs.

4. The method of claim 3, further comprising forming a number of other vias, each of the other vias extending through the dielectric layer and one of the insulating plugs, wherein each of the other vias extends to the one conductor in the second interconnect structure associated with the one insulating plug.

5. The method of claim 4, further comprising:
forming a number of trenches in the dielectric layer, each trench located coincident with one of the other vias; and
depositing a conductive material in each of the other vias and each of the trenches, the conductive material in each of the trenches forming a land.

6. The method of claim 5, wherein the conductive material comprises a copper material.

7. The method of claim 5, further comprising depositing a connection element on each of the lands.

8. The method of claim 5, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the trenches.

9. The method of claim 4, further comprising depositing a conductive material in each of the other vias.

10. The method of claim 9, wherein the conductive material comprises a copper material.

11. The method of claim 9, further continuing deposition of the conductive material to form connection elements proximate at least some of the other vias.

12. The method of claim 1, wherein the insulating material comprises an oxide material.

13. The method of claim 12, wherein the insulating material comprises SiO_2.

14. The method of claim 1, wherein the insulating material comprises one of a nitride material, a carbide material, and a polymer material.

15. The method of claim 1, further comprising cutting the wafer stack into a plurality of stacked die.

16. The method of claim 15, further comprising packaging one of the stacked die to form a packaged integrated circuit device.

17. The method of claim 1, further comprising forming at least one dummy via extending through the first interconnect structure and into the first wafer.

18. A method comprising:
forming a first interconnect structure on one side of a first wafer;
forming a number of vias, each of the vias extending through the first interconnect structure and into the first wafer;
depositing a layer of insulating material over a surface of each of the number of vias;
depositing a sacrificial material on the insulating layer in each of the number of vias;
forming a second interconnect structure over the first interconnect structure, wherein the sacrificial material in each of the number of vias extends to one of a number of conductors in the second interconnect structure; and
bonding the first wafer to a second wafer to form a wafer stack.

19. The method of claim 18, further comprising:
thinning an opposing side of the first wafer to expose the sacrificial material within each of the vias.

20. The method of claim 19, further comprising performing alignment of the wafer stack using the exposed vias and sacrificial material.

21. The method of claim 19, further comprising depositing a layer of dielectric material over the opposing side of the first wafer and the exposed vias.

22. The method of claim 21, further comprising:
forming a number of other vias, each of the other vias extending through the dielectric layer and to the sacrificial material in one of the number of vias; and
removing the sacrificial material from each of the number of vias, wherein each of the vias extends to one of a number of conductors in the second interconnect structure.

23. The method of claim 22, further comprising:
forming a number of trenches in the dielectric layer, each trench located coincident with one of the other vias; and
depositing a conductive material in each of the vias and each of the trenches, the conductive material in each of the trenches forming a land.

24. The method of claim 23, wherein the conductive material comprises a copper material.

25. The method of claim 23, further comprising depositing a connection element on each of the lands.

26. The method of claim 23, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the trenches.

27. The method of claim 22, further comprising depositing a conductive material in each of the vias.

28. The method of claim 27, wherein the conductive material comprises a copper material.

29. The method of claim 27, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the vias.

30. The method of claim 22, wherein the sacrificial material comprises one of a glass material and a polymer material.

31. The method of claim 22, wherein removing the sacrificial material comprises performing an etching process.

32. The method of claim 31, wherein the etching process is performed using a solution that removes the sacrificial material at a faster rate than the dielectric material.

33. The method of claim 18, further comprising:
etching an opposing side of the first wafer to expose the layer of insulating material in each of the vias.

34. The method of claim 33, further comprising performing alignment of the wafer stack using the exposed vias and insulating material.

35. The method of claim 33, further comprising depositing a layer of dielectric material over the opposing side of the first wafer and the exposed insulating material.

36. The method of claim 35, further comprising:
forming a number of trenches in the dielectric layer and the exposed insulating material to expose the sacrificial material; and
removing the sacrificial material from each of the number of vias, wherein each of the vias extends to one of a number of conductors in the second interconnect structure.

37. The method of claim 36, further comprising depositing a conductive material in each of the vias and each of the trenches.

38. The method of claim 37, wherein the conductive material in each of the trenches forms a land, the method further comprising depositing a connection element on each of the lands.

39. The method of claim 37, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the trenches.

40. The method of claim 18, wherein the insulating material comprises one of an oxide material, a nitride material, and a carbide material.

41. The method of claim 40, wherein the insulating material comprises one of SiO_2, Si_3N_4, and SiC.

42. The method of claim 18, further comprising cutting the wafer stack into a plurality of stacked die.

43. The method of claim 42, further comprising packaging one of the stacked die to form a packaged integrated circuit device.

44. The method of claim 18, further comprising forming at least one dummy via extending through the first interconnect structure and into the first wafer.

45. A method comprising:
forming a first interconnect structure on one side of a first wafer;
forming a number of vias, each of the vias extending through the first interconnect structure and into the first wafer;
depositing a layer of insulating material over a surface of each of the number of vias;
depositing a conductive material on the insulating layer in each of the number of vias;
forming a second interconnect structure over the first interconnect structure, wherein the conductive material in each of the number of vias extends to one of a number of conductors in the second interconnect structure; and
bonding the first wafer to a second wafer to form a wafer stack.

46. The method of claim 45, further comprising:
thinning an opposing side of the first wafer to expose the conductive material within each of the vias.

47. The method of claim 46, further comprising performing alignment of the wafer stack using the exposed vias and conductive material.

48. The method of claim 46, further comprising depositing a layer of dielectric material over the opposing side of the first wafer and the exposed vias.

49. The method of claim 48, further comprising forming a number of other vias, each of the other vias extending through the dielectric layer and to the conductive material in one of the number of vias.

50. The method of claim 49, further comprising:
forming a number of trenches in the dielectric layer, each trench located coincident with one of the other vias; and
depositing a conductive material in each of the other vias and each of the trenches, the conductive material in each of the trenches forming a land.

51. The method of claim 50, wherein the conductive material in each of the vias and the conductive material in each of the other vias comprises a copper material.

52. The method of claim 50, further comprising depositing a connection element on each of the lands.

53. The method of claim 50, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the trenches.

54. The method of claim 49, further comprising depositing a conductive material in each of the other vias.

55. The method of claim 54, wherein the conductive material in each of the vias and the conductive material in each of the other vias comprises a copper material.

56. The method of claim 54, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the other vias.

57. The method of claim 45, further comprising:
etching an opposing side of the first wafer to expose the layer of insulating material in each of the vias.

58. The method of claim 57, further comprising performing alignment of the wafer stack using the exposed vias and insulating material.

59. The method of claim 57, further comprising depositing a layer of dielectric material over the opposing side of the first wafer and the exposed insulating material.

60. The method of claim 59, further comprising forming a number of trenches in the dielectric layer and the exposed insulating material to expose the conductive material in the vias.

61. The method of claim 60, further comprising depositing a conductive material in each of the vias and each of the trenches.

62. The method of claim 61, wherein the conductive material in each of the trenches forms a land, the method further comprising depositing a connection element on each of the lands.

63. The method of claim 61, further comprising continuing deposition of the conductive material to form connection elements proximate at least some of the trenches.

64. The method of claim 45, wherein the insulating material comprises one of an oxide material, a nitride material, and a carbide material.

65. The method of claim 64, wherein the insulating material comprises one of SiO_2, Si_3N_4, and SiC.

66. The method of claim 45, further comprising cutting the wafer stack into a plurality of stacked die.

67. The method of claim 66, further comprising packaging one of the stacked die to form a packaged integrated circuit device.

68. The method of claim 45, further comprising forming at least one dummy via extending through the first interconnect structure and into the first wafer.